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Finite Element Analysis of Dependence of Programming Characteristics of Phase-Change Memory on Material Properties of Chalcogenides

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The programming characteristics of a phase-change memory (PCM) cell with a chalcogenide layer contacted by a resistive heater are investigated by finite element modelling. As analyzed in this study, the characteristics are markedly affected by the resistivity of the phase-change chalcogenide material. A higher reset current of 1.6 mA is required for the as-fabricated virgin PCM than that of 1.3 mA for the cycled PCM because of the resistivity difference of the chalcogenides in the two cases. More importantly, a chalcogenide layer with a much higher resistivity than the resistive heater is necessarily adopted for a higher energy efficiency to markedly reduce reset current to 0.6 mA or even lower while slightly increasing reset voltage.
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KEYWORDS: material properties, programming characteristics, PCM, low reset current, finite element analysis

1. Introduction

Owing to the limitations of the today's widespread flash memory, it is necessary to develop candidates for next-generation nonvolatile memories (NVMs).[1–3] Phase-change memory (PCM) has exhibited many advantages so that it is widely regarded as the best candidate. PCM technology is based on a reversible local structural switching between the amorphous and crystalline phases of chalcogenide alloys [e.g., $Ge_2Sb_2Te_5$ (GST)].[4–8] The switching is induced by Joule heating due to current flow.

The high reset amorphization current of existing PCMs, for instance, about 1–2 mA at the 180 nm node for a conventional normal-bottom-contact (NBC) cell, is one of biggest barriers for its mass production.[9,10] We previously proposed a confined-chalcogenide (CC) cell structure for reducing this current.[11] As we analyzed by finite element modelling, the reset operation of a CC cell is possible at about 0.8 mA, which is much lower than that of the NBC cell. Although there are other approaches to reducing reset current by the adopting an edge-contact or so-called μ-trench PCM structure, very complicated fabrication processes and large cell sizes for these cells would be necessary compared with those for the NBC cell.[12] The contact area between the chalcogenide layer and the bottom resistive heater could be decreased markedly by adopting an electron beam or a focused ion beam to define pore size, resulting in a much lower reset current.[13,14] However, these methods are used to investigate the scalability of a PCM memory or to demonstrate the possibility of a low operation current by decreasing the contact area between the chalcogenide layer and the contact electrode.

The simple configuration and high scalability of the NBC cell make it very promising compared with other structures. Materials properties, particularly the resistivity of the chalcogenide, are expected to have a marked effect on the operation current of PCM. To determine the effect, in this study we analyze the dependence of material properties on the programming characteristics of an NBC cell by finite element modelling. As we will report, the reset current of an as-fabricated virgin PCM is slightly higher than that of a PCM in the cycled period. The reset current can be markedly decreased by adopting a chalcogenide material with a much higher resistivity than a resistive heater.

2. Resistivities of GST Chalcogenides in PCM

As generally known, GST is crystallized owing to the passivation process at about 400 °C during metal contact formation upon completion of device fabrication. This process could decrease resistivity of GST to approximately 2 mΩ·cm. Here, we call such a state the as-fabricated virgin set state.

On the other hand, when a PCM cell enters its cycled period, the programmable region is reversibly structure-switched between amorphous and face-centered-cubic (fcc) crystalline phases.[16] As previously reported by our group and other research groups, the fcc crystalline phase has a resistivity of approximately 10 mΩ·cm.[8,15]

Furthermore, as shown in Fig. 1, our experimental results indicate that the resistivity of crystalline GST (c-GST) increases by up to two or three orders of magnitude with the nitrogen concentration in the GST, which can be easily controlled by adjusting the flow ratio of N_2 gas to Ar gas during sputtering.

As a result, the resistivity of GST chalcogenides varies depending on the operation history or doping concentration of chalcogenides. The programming characteristics of PCM should be strongly affected by material properties such as

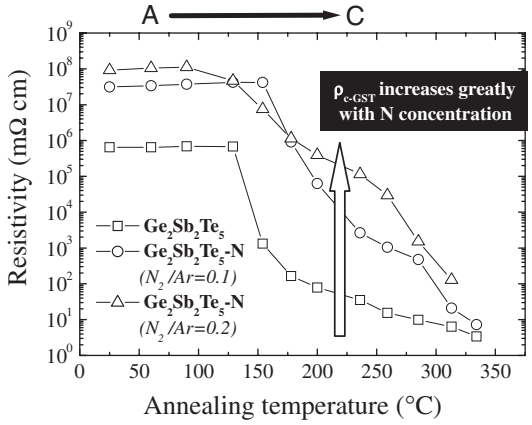

Fig. 1. Resistivity as function of annealing temperature. Resistivity could be controlled by simply changing the flow ratio of N_2 gas to Ar gas.

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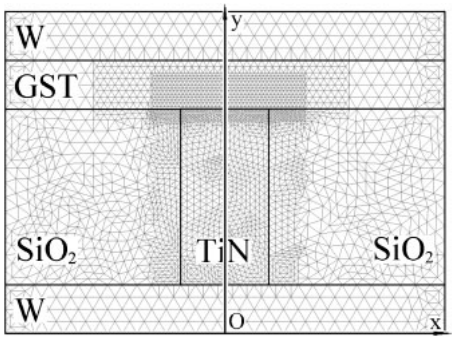

Fig. 2. Meshed finite element modelling of single normal-bottom-contact PCM cell structure.

resistivity because the programming of PCM is based on Joule heating. In the following sections we will investigate such an effect by finite element modelling of NBC PCM cells.

3. Finite Element Modelling of PCM

The mathematical model for heat transfer by conduction is the heat equation

$$\rho C \frac{\partial T}{\partial t} - \nabla \cdot (k \nabla T) = Q, \tag{1}$$

where ρ is the density, T is the temperature, C is the heat capacity, k is the thermal conductivity, t is the time and Q is the heat flux.

The heat generated by Joule heating Q is given by

$$Q = \frac{1}{\sigma} |J|^2 = \sigma |\nabla V|^2, \tag{2}$$

where σ is the electric conductivity, J is the electric current density and V is the electric potential.

Equation (1) is solved in this study by finite element analysis using the commercially available software COMSOL 3.2. Figure 2 shows the meshed finite element modelling of the PCM cell structure analyzed in this study. Chalcogenide GST is chosen as a phase-change material here. SiO_2 is adopted for the thermal isolation of the resistive heater TiN and the programmable GST region. The NBC PCM cell is assumed to have a bottom W/TiN resistive heater/GST/top W layered structure, and the thicknesses of layers, from bottom W, are 100, 360, 100, and 100 nm. The TiN heater is 180 nm in width. The coordinates are shown in Fig. 2, in which the x-axis is along the bottom surface of the bottom W and the y-axis is along the centerline of the memory cell. Refine meshes were applied to important regions of both the resistive heater TiN and GST chalcogenide layers for a more accurate simulation of temperature distribution in the cell. The required thermal and electrical properties of the materials used in the simulation are given in Table I.

In this study, all of the exterior boundaries are set at room temperature (298 K) and all of the interior boundaries are set as continuous boundary conditions. As described in ref. 10, the junction temperature T_J reaches 353 K at a 3.3 or 5 V operation voltage in microelectronics and the top of the W layer remains at room temperature (298 K). For simplification, it is reasonable to set the top and bottom boundaries of the PCM cell at room temperature in this study because there is a very small effect on the temperature distribution and programming characteristics.

Table I. Physical properties of materials used in simulation.

Material	Density ρ (kg/m^3)	Specific heat C (J/kg K)	Thermal cond. k (W/m K)	Resistivity ρ_e (Ω m)
c-GST	6200	202	0.46	$\rho_{\text{c-GST}}$ (Doping dependent)
a-GST	6200	202	0.46	$10^4 \times \rho_{\text{c-GST}}$
Heater	5240	784	0.44	1.2×10^{-4}
W	19300	132	174	5.39×10^{-8}
SiO_2	2330	1330	1.4	1×10^{14}

The following assumptions for the simplification of the simulation are also taken into account: (1) The temperature dependences of the thermal and electrical properties of the materials are neglected. (2) The electrical pulses applied to the PCM cell are exact square waveforms, neglecting the rising and falling edges of the pulses. (3) The melting point increase with the concentration of nitrogen doped into GST is neglected. (4) The latent heat of fusion of GST is neglected.

4. Simulation Results and Discussion

Figures 3(a), 3(c), and 3(e) show the thermal and heat flux distributions just after the application of a programmable current pulse of 1.2 mA and 30 ns in the three cases of the c-GST resistivities of 2, 10, and 100 mΩ·cm, respectively. The c-GST resistivities are about one order of magnitude lower, close to and about one order of magnitude higher than that of the resistive heater (12 mΩ·cm[15]), respectively. Figures 3(b), 3(d), and 3(f) show the temperature profiles in the on-current period along the y-axis in the above three cases, respectively.

Under actual conditions, an electrical pulse of about 1–2 mA and about 10–100 ns is usually applied to a memory cell for the reset operation in the case of the c-GST resistivity of 10 mΩ·cm. However, for easy comparison, an identical pulse of 1.2 mA and 30 ns is adopted in all of the above three cases although the temperature is extremely high in the case of the c-GST resistivity of 100 mΩ·cm. This is because part of the SiO_2 layer surrounding TiN and GST in this case would reach its melting point of approximately 1900 K according to the corresponding temperature distribution, resulting in device failure. In actual operations, we certainly should operate at a current that makes the temperature of the programmable GST region is only slightly higher than its melting point.

It is clearly observed from Fig. 3(a) that the high-temperature bright region is in the resistive heater. The maximum temperature is almost located at the center of the heater. The interface between the GST layer and the heater is in the medium-temperature region. Figure 3(c) shows that part of the high-temperature region is already located in the GST/TiN contact region. The bright high-temperature region in Fig. 3(c) moves upward compared with that in Fig. 3(a). Figure 3(e) clearly shows that the high-temperature region is mainly located in the GST layer rather than in the resistive heater, as in Figs. 3(a) and 3(c).

The detailed temperature profiles along the centerline of

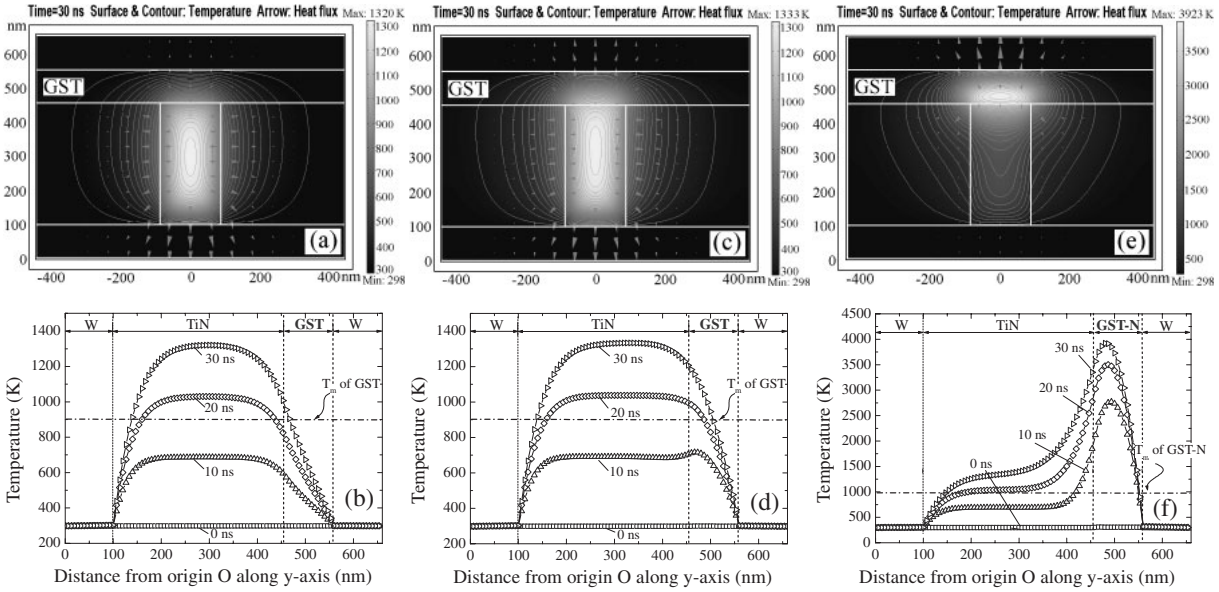

Fig. 3. (a), (c), and (e) Temperature and heat flux distributions at electrical pulse of 1.2 mA and 30 ns when c-GST has relatively low resistivity of 2 mΩ·cm, resistivity of 10 mΩ·cm and relatively high resistivity of 100 mΩ·cm, respectively. (b), (d), and (f) Temperature profile changes for various times along centerline of cell structure, corresponding to (a), (c), and (e), respectively.

the cell structure for various times in the on-current period are shown in Figs. 3(b), 3(d), and 3(f), corresponding to Figs. 3(a), 3(c), and 3(e), respectively. The temperature increases almost linearly at the center of the TiN heater. At 30 ns, a very small amount of GST above the interface between the GST layer and the heater could be melted, as shown in Fig. 3(b). On the other hand, the temperature for most of the GST above the interface is high than the melting point of GST in Fig. 3(f).

As observed from the temperature distributions in Fig. 3, heat almost fluxes vertically and the left and right exterior boundaries of the analyzed PCM cells remain at room temperature immediately after electric current is cut off. This indicates that setting these boundaries at room temperature has almost no effect on programming characteristics.

Figures 4(a) and 4(b) show that temperature profiles of PCM cells with GST layers of various resistivities along the centerline of the cell structure and on the GST bottom surface, respectively. Comparing these temperature profiles, we observe that the resistivity of c-GST has a marked effect on the temperature profiles. When the resistivity of c-GST is much lower and higher than that of TiN, the local temperature increase of the GST layer above the interface is caused mainly by thermal transfer from the heater and self-Joule-heating in GST, respectively. When the resistivity of c-GST is close to that of TiN, the temperature increase of GST is caused by both thermal transfer and self-Joule-heating in GST.

At the same current, the temperature in the cycled case is obviously higher than that in the virgin case on the basis of the above simulation analysis. To reach the same temperature, a higher current is necessary for the latter case. Therefore, the cycled reset current is lower than the virgin reset current as observed from the simulation results on the reset current and reset voltage as functions of the resistivity of c-GST in Fig. 5, in which the former and the latter are about 1.3 and 1.6 mA, respectively. The inset of Fig. 5 shows the detailed simulation results of device resistance vs programming current when the resistivity of c-GST is varied.

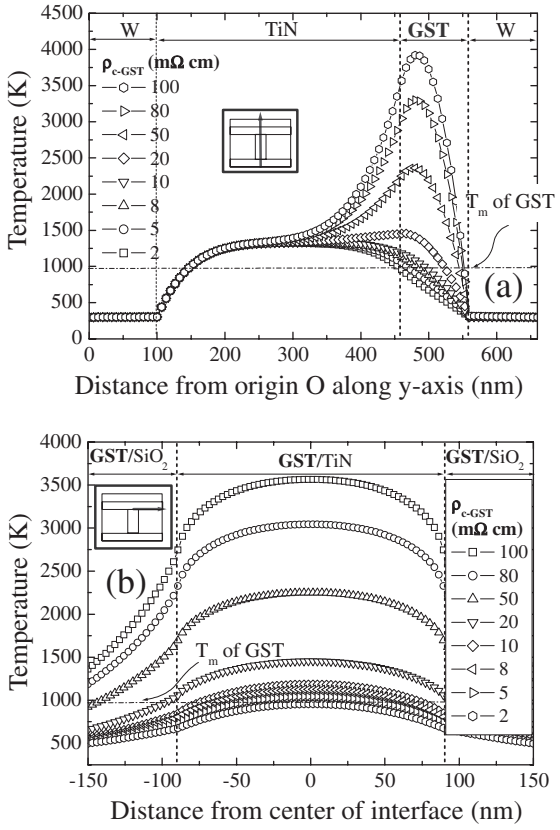

Fig. 4. Temperature distributions parameterized in resistivity of GST (a) along centerline of the cell structure and (b) on bottom surface of GST layer for programming for reset state at an electrical pulse of 1.2 mA and 30 ns.

As shown in Fig. 5, we note that reset current could be

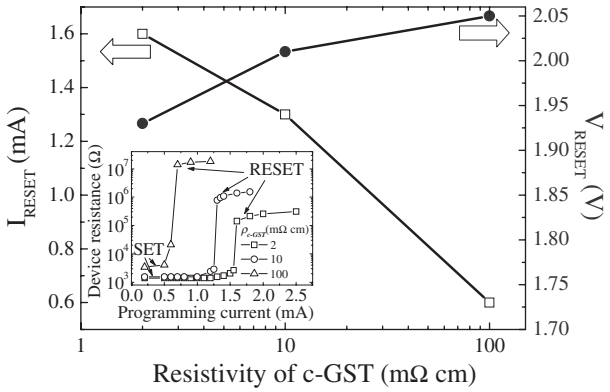

Fig. 5. Reset current and corresponding reset voltage as function of resistivity of c-GST. The inset shows the detailed simulation results of device resistance vs programming current.

markedly decreased when the resistivity of c-GST is much larger than that of the resistive heater (or the small contact electrode). As shown in the inset of Fig. 5, the device resistance of the PCM cell in the set state includes the resistance of the resistive heater and does not increase linearly with the resistivity of chalcogenide in the range of 0.2–100 mΩ·cm at all. Thus, the corresponding reset voltage, however, slightly increases with the resistivity of chalcogenide. The reset voltages of PCM in the three cases of the resistivities of crystalline GST of 2, 10, and 100 mΩ·cm are 1.93, 2.01, and 2.05 V, respectively. As a consequence, adopting c-GST with a higher resistivity than contact electrodes could markedly increase the energy efficiency by self-Joule-heating in GST instead of thermal transfer from the heater.[17] Increasing the resistivity of c-GST is realizable by doping nitrogen into GST, as shown in Fig. 1. There are also other approaches to increasing the resistivity of chalcogenide. One can dope other elements such as oxygen and silicon into the GST film.[18] Incorporating SiO_2 or other dielectrics into the GST film using cosputtering could also increase the resistivity of chalcogenide to reduce the reset current.[13,19]

5. Conclusions

The resistivity ratio of the GST chalcogenide to the resistive heater has a marked effect on the temperature profiles of PCM. Thermal transfer and self-Joule-heating mainly contribute to a local temperature increase in a GST layer when the resistivity of c-GST is much lower and higher than that of TiN, respectively. When the resistivity of c-GST is close to that of TiN, the temperature increase is caused by both thermal conduction and self-Joule-heating. The cycled reset current should be slightly lower than the virgin reset current. To lower the reset current, it is better to adopt a phase-change material that has a higher resistivity than the small contact electrode.

Acknowledgments

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